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| D:\UAAR\UIIT\courseOutlineCommittee\CourseContents_Final_V02\New folder\logo4.png | **PMAS Arid Agriculture University Rawalpindi**  **University Institute of Information Technology** | | | | C:\Users\Shahid\Downloads\IMG-20210824-WA0001.jpg |
| **CS-530 Computer Organization and Assembly Language** | | | | | | |
| **Credit Hours:** | | **4(3-3)** | **Prerequisites:** | **(CS-430)** | | |
| **Teacher:** | |  |  |  | | |
| **Course Description:** | | | | | | | |
| Difference between Architecture and Organization, Components of Computer and Busses, Structure and Function of Computer, The Von Neumann Machine, Structure and Expanded Structure of IAS Computer, Fundamental Computer Elements (Gate and Memory cell), The Evolution Of The Intel X86 Architecture, Computer Components: Top-Level View, Instruction Fetch and Execute, Instruction Cycle State Diagram, Interrupts and Transfer of Control with Multiple Interrupts, Instruction Cycle with Interrupts, Instruction Cycle State Diagram, with Interrupt, Interconnection structure (CPU Module with signal lines, Memory Module with signal lines, I/O Module with signal lines, Bus Interconnection, Bus Structure, Typical control lines/signals, Multiple-Bus Hierarchies, Traditional bus organization and architecture), PCI bus organization and Architecture, Computer Memory Systems, Characteristics of Memory Systems, The Memory Hierarchy, Cache/Main Memory Structure, Cache Read Operation, ROM Memory, Design of ROM, Types of ROM, RAM Memory, Design of RAM, Types of RAM, I/O Modules, Programmed I/O, Interrupt-Driven I/O, Direct Memory Access, Instruction Set Design, Addressing, x86 Addressing Modes, Instruction Cycle, MIPS and 8088 Assembly Language Programming | | | | | | | |
| **Course Objective:** | | | | | | | |
| Modern computer technology requires professionals of every computing specialty to understand both hardware (HW) and software (SW). The interaction between HW and SW also offers a framework for understanding the fundamentals of computing. This course will have HW focus in the class and students will study topics such as Instruction Set Architecture, Basic Assembly Instructions, Addressing Modes, Computer Performance evaluation, Floating Point Data, Data Path Design for Single Cycle and Multiple Cycle Computers, Pipelined Data Path Basics, Hazards in Pipelining, Memory hierarchy design, storage and I/O. The Lab will have focus on MIPS and 8088 Assembly Level Programming and someHW experiments. The course will have one comprehensive design project in which students will design and implement an 8-bit MIPS or 8088 architecture-based processor using HWcomponents (preferably). | | | | | | | |
| **Teaching Methodology:** | | | | | | | |
| Lectures, Written Assignments, Practical labs, Semester Project, Presentations | | | | | | | |
| **Courses Assessment:** | | | | | | | |
| Mid Exam, Home Assignments, Quizzes, Project, Presentations, Final Exam | | | | | | | |
| **Reference Materials:** | | | | | | | |
| * “Computer Organization and Architecture” by William Stallings (10thEdition) * Assembly Language for Intel® Based Computers - Fifth Edition, Kip Irvine * Computer Organization & Design: The Hardware/Software Interface by Patterson & Hennessy, Morgan & Kauffman Series 5thEdition. | | | | | | | |

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| **Course Learning Outcomes (CLOs):** | | |
| At the end of the course the students will be able to: | **Domain** | **BT Level\*** |
| 1. Acquire the basic knowledge of computer organization, computer architecture and assembly language | C | 1 |
| 1. Understand the concepts of basic computer organization, architecture, and assembly language techniques | C | 2 |
| 1. Solve the problems related to computer organization and assembly language | C | 2 |
| \* BT= Bloom’s Taxonomy, C=Cognitive domain, P=Psychomotor domain, A= Affective doma | | |

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| **Week/Lecture #** | | **Theory** | | **Practical** |
| Week 1 | Lect-I | What is the Architecture of Computer?  Why Study Computer Organization  Difference between Architecture and Organization | | What is assembly language  Installing of MASM compiler  Different commands of MASM compiler |
| Lect-II | Components of Computer and Busses, Structure and Function of computer | |  |
| Week 2 | Lect-I | The Von Neumann Machine  Structure and Expanded Structure of IAS Computer | | Brief history of X86  What is segmentation and its types, Syntax of Assembly Language Program |
| Lect-II | Fundamental Computer Elements (Gate and Memory cell)  The Evolution of The Intel X86 Architecture | |  |
| Week 3 | Lect-I | Computer Components: Top-Level View  Instruction Fetch and Execute  Instruction Cycle State Diagram | | Instruction Cycle State Diagram, with Interrupt |
| Lect-II | Interrupts and Transfer of Control with Multiple Interrupts  Instruction Cycle with Interrupts | |  |
| Week 4 | Lect-I | Interconnection structure  CPU Module with signal lines  Memory Module with signal lines  I/O Module with signal lines, Bus Interconnection, Bus Structure | | First Assembly Program  MOV & ADD instructions  Logical Vs Physical Addressing, Flag Register |
| Lect-II | Typical control lines/signals, Multiple-Bus Hierarchies, Traditional bus organization and architecture | |  |
| Week 5 | Lect-I | High-performance bus organization and architecture, Elements of Bus Design, PCI bus organization and Architecture | | Assembly Language Fundamentals, Unsigned Addition, Multiplication, Subtraction and Addition |
| Lect-II | Computer Memory Systems, Characteristics of Memory Systems  The Memory Hierarchy | |  |
| Week 6 | Lect-I | Cache/Main Memory Structure  Cache Read Operation | | Defining Data  Data Types, Labels |
| Lect-II | Typical Cache Organization  Elements of Cache Design | |  |
| Week 7 | Lect-I | Cache Addresses, Cache Mapping Function, Cache Write Policy | | Jumps and its types |
| Lect-II | ROM Memory, Design of ROM, Types of ROM | |  |
| Week 8 | Lect-I | RAM Memory | | Analysis of Few Assembly Programs |
| Lect-II | Design of RAM  Types of RAM | |  |
| **Mid Term Exam** | | | | |
| Week 9 | Lect-I | I/O Modules  Programmed I/O | Loops using Loop keyword and using backward jump | |
| Lect-II | Interrupt-Driven I/O  Direct Memory Access |  | |
| Week 10 | Lect-I | Elements of a Machine Instruction  Instruction Representation  Instruction Types | Subroutines and Call statement | |
| Lect-II | Number of Addresses and Address SchemesInstruction Set Design |  | |
| Week 11 | Lect-I | MIPS Architecture | MIPS assembly | |
| Lect-II | MIPS ISA |  | |
| Week 12 | Lect-I | Types of Operands  Intel x86 and MIPS Data Types | Arrays in assembly language  Stack | |
| Lect-II | Types of Operations, Data Transfer |  | |
| Week 13 | Lect-I | Types of Operands  Intel x86 and ARM Data Types |  | |
| Lect-II | Types of Operation, Data Transfer |  | |
| Week 14 | Lect-I | Addressing, Immediate Addressing  Direct Addressing, Indirect Addressing | x86 and ARM Addressing Modes | |
| Lect-II | Register Addressing  Register Indirect Addressing  Displacement Addressing  Stack Addressing |  | |
| Week 15 | Lect-I | Instruction Formats  x86 and ARM Instruction Formats | Example Microprocessor Register Organizations | |
| Lect-II | Processor Organization  Register Organization |  | |
| Week 16 | Lect-I | Instruction Cycle, The Indirect Cycle, Data Flow, Instruction Pipelining, Dealing with Branches | Project Demo and Presentation | |
| Lect-II | Project Demo and Presentation |  | |
| **Final Term Exam** | | | | |